**SRM Institute of Science and Technology**

**Department of Computer Science and Engineering**

**Subject Title: Computer Organization and Architecture**

**Subject code: 18CSC203J**

**CT2Questions Date: 19.10.2020 Time: 9.00 a.m. to 10.30 a.m.**

**MARKS (50)**

**SECTION A (EASY)(20\*1=20)**

1.

When adding two signed n-bit numbers, the \_\_\_\_\_\_\_\_\_ signal is ignored from MSB position.

A. carry out

B. carry in

C. positive

D. Negative

ANSWER: A

2

.………….. reduces the number of summands by a factor of 2.

A. Bit pair recoding

B. Binary pair recoding

C. Singe bit recoding

D. Multiple pair recoding

ANSWER: A

3.

The ……..representation of numbers occupies a large amount of memory.

A. 1’s complement

B. 2’s complement

C. signed numbers

D. Signed magnitude

ANSWER: D

4

A nibble is a group of ……. bits

A. 16

B. 8

C. 4

D. 2

ANSWER: C

5.

In sequential binary multipliercircuit,multiplier bit is stored in \_\_\_\_\_ .

A. A register

B. Shift register

C. M register

D. n-bit adder

ANSWER: B

6

. ………is/are used to implement the sum circuit using full adders.

A. AND & OR Gates

B. NAND gate

C. XOR

D. XNOR

ANSWER: C

7

. …………… is used in decimal numbers when a value is written to the power of 10.

A. Height factors

B. Size factors

C. Scale factors

D. Form Factors

ANSWER: C

8.

The multiplication is implemented using ……….

A. Flip flops

B. Combinatorial

C. Fast adders

D. Full adders

ANSWER: C

9.

Value represented in single precision is \_\_\_\_\_\_\_\_\_.

A.+/- 1.M \*2^E’-127

B.+ 1.M\*2^E’-126

C. + 1.M\*2^E’-125

D. - 1.M\*2^E’-127

Answer: A

10.

\_\_\_\_\_ is the size of mantissa in Double Precision IEEE standard floating-point format.

A.10-bit

B.11-bit

C.23-bit

D.52-bit

Answer:D

11.

The instruction fetch unit has executed branch instruction concurrently with execution of other instruction is termed as

A. Branch folding

B. Prediction

C.Delayed branching

D.Static prediction

Answer: A

12.

The conditional branch instruction outcome can be predicted before the execution by using a logic called

A.Branch prediction

B.Delayed branch

C.Structural hazard

D.Static prediction

Answer: A

Y, temp and Z in single bus organization refers to

1. General purpose registers used by the processor
2. Temporary registers used by processor
3. Accumulator
4. Special purpose registers used by processor

Answer: B

Prediction decision may change depending on the execution history is

1. Static prediction
2. Dynamic prediction
3. Branch instruction
4. Penalty

Answer: **B**

15.

A technique which is used to minimize the penalty caused by conditional branch is \_\_\_\_\_\_\_\_\_\_

1. Delayed branching
2. Branch penalty
3. Delay
4. Prediction

Answer: A

16.

Operand forwarding method doesthe following to overcome data dependencies

A. Introduce NULL instructions  
B. Result of the instruction is written to the temporary register **C.**Result of one instruction is directly sent to the next instruction for execution

D. Blocking the execution of instructions

Answer: C

17.

When the control signal RUN is set to 1 in hardwired control systems

A. The counter is to be incremented by 1 at the end of every clock cycle

B. The counter is to be incremented by 2 at the end of every clock cycle

C. The counter is to be incremented by 3 at the end of every clock cycle

D. The counter is to be incremented by 4 at the end of every clock cycle

Answer: A

Which addressing mode is capable of working without fetch operation?

1. Register indirect
2. Direct
3. Indexed
4. Immediate

Answer: D

Which of the following cannot be a condition code?

1. Overflow
2. Zero result
3. Positive result
4. Negative result

**Answer: c**

20.

Which of the following statement is true with respect to the function of WMFC signal?

1. Used to make processor wait for the reply from memory
2. Execution of memory instructions
3. Idle state of memory
4. No operation

Answer: A

**Section B (MEDIUM)( 15\*1=15)**

1.

In binary division, A and Q registers are shifted by \_\_\_\_\_\_.

A. right one binary position

B. left one binary position

C. left two binary positions

D. right two binary positions

ANSWER: B

2.

The sum of the two binary numbers, 0110 & 0110 is …….

A. 1100

B. 1111

C. 1001

D. 1010

ANSWER: A

3.

The function*ci + 1 = yici + xici + xiyi*is a carry generation implemented in \_\_\_\_\_\_\_\_\_\_\_\_.

A. Half adders

B. Full adders

C. Ripple adders

D. Fast adders

ANSWER: B

4.

Multiplier bit-pair recoding table, under which condition multiplicand selected at

Position i is -2\*M.

A. 1 0 1

B. 1 0 0

C. 0 1 1

D. 1 1 0

Answer: B

5.

…….. is the recoding of the multiplier -6(11010)

A. 0-1-2

B. 0-1+1-10

C. -2-10

D. 0+1-1-10

ANSWER: A

6.

Innon-restoring division algorithm, for Dividend=1000 and Divisor=100. How many cycles are required to get the correct division result?

A.4

B.5

C.3

D.6

Answer:A

7.

What is the relation between sign exponent E and bias exponent E’ in single precision floating point number?

A.E=E’-1023

B.E=E’+127

C.E=127-E’

D.E=E’-127

Answer:A

The relation between the performance of the pipeline and the no. of stages used in the pipeline are--------------------

1. Directly proportional
2. Inversely proportional
3. No relation between them
4. None

**Answer: a**

9.

What is the reason for incrementing the PC by 4 in multi-bus organization?

A. The word size is 8 bit

B. The word size is 16 bit

C. The word size is 32 bit

D. The word size is 64 bit

**Answer: C**

**10.**

The function of Rin is to

A. load the data from bus to register

B. place the content of register onto the bus

C. fetch the data

D. execute the data

Answer: A

11.

Add #X, R1, R2. This instruction performs the operation

1. R1<- X+[R2]
2. R1->X+[R2]
3. R2<-X+[R1]+[R2]
4. R2<-X+[R1]

Ans : d) R2<-X+[R1]

**12.**

**.**

The above sequence of opertations represents

1. R3=R1+R2
2. R1=R2+R3
3. R2=R1+R3
4. R3=R2-R1

Answer: A

13.

Which expression gives the offset value?

A.Offset= (address immediately following the branch instruction)-(branch target address )

1. Offset=address immediately following the branch instruction-(PC)

C. Offset=(PC)-(address immediately following the branch instruction)

D. Offset= (branch target address) – (address immediately following the branch instruction.)

**Answer: D**

14.

How many buffers are required in the Hardware organization for 2 stage pipeline and4 stage pipeline?

A. 2, 1

B. 1, 3

C. 3, 1

D. 2, 4

Answer: B

If the state machine moves from LNT to LT in two stage algorithm then

A. branch is taken

B. branch is not taken

C. branch is strongly taken

D. branch is strongly not taken

Answer: A

**Section C DIFFICULT (5\*1=5)**

1.

What is the result of IEEE double precision representation for (1259.125)?

A.0100000010010011101011001....

B.1100000010010011101011001....

C.1111000010010011101011001....

D.0100001110010011101011001....

Answer: A

2.

Innon-restoring division algorithm, after performing left shift operation on A, Q registers, if magnitude of A < 0 then?

A.Q0=0, A=A+M

B.A=A+M

C.Q0=1

D.A=A-M

Answer: B

3

. …….. is the Booth recoded multiplier bit of the multiplier 11010

A. 0 -1 -1 0 0

B. 0 -1 +1 +1 0

C. 0 -1 +1 -1 0

D. 0 +1 -1 -1 0

ANSWER: C

4.

Let there be two instructions I1 and I2 such that:  
I1 : ADD R1, R2, R3  
I2 : SUB R4, R1, R2

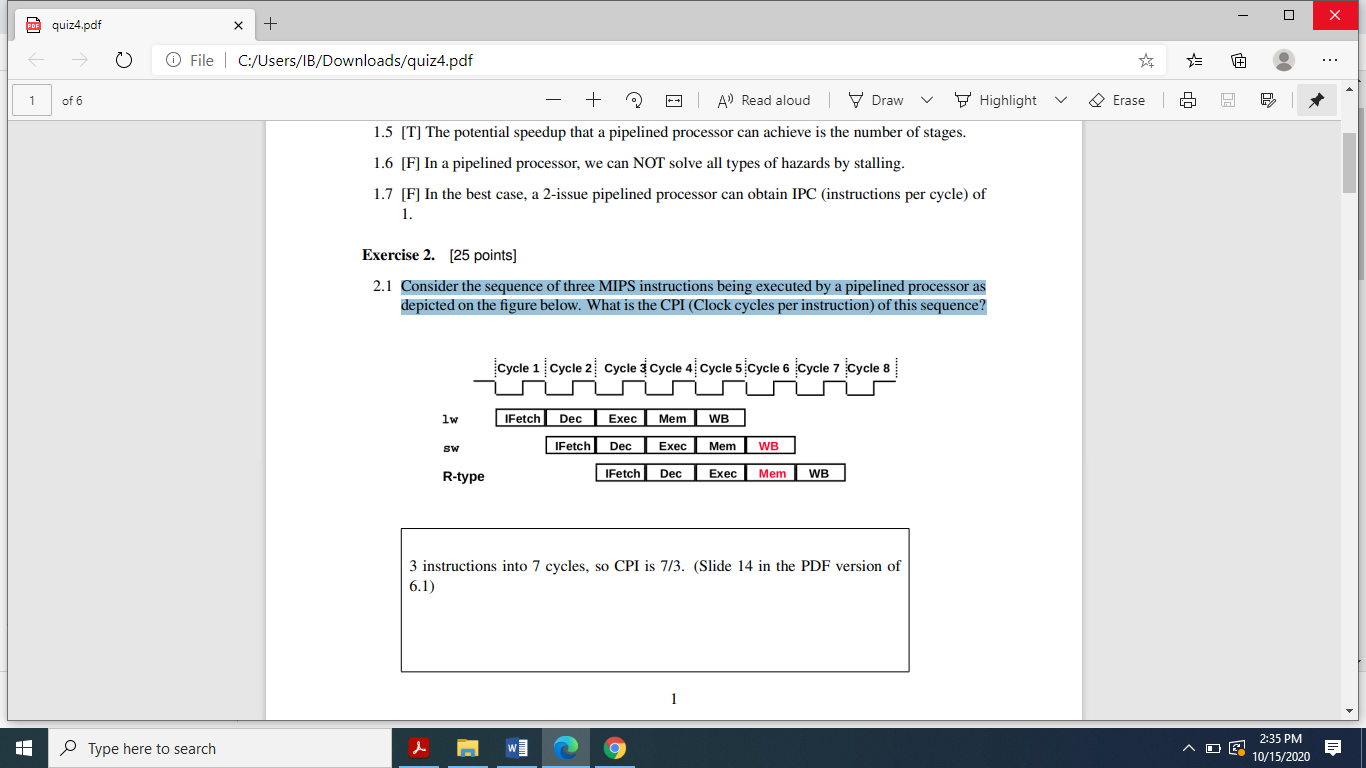
Identify the type of hazard which occurs in the above instruction

1. Structural hazard
2. Data hazard
3. Control hazard
4. Instructional hazard

Answer: Data hazard

5.

Consider the sequence of three MIPS instructions being executed by a pipelined processor as depicted on the figure below. What is the CPI (Clock cycles per instruction) of this sequence?



1. 7/3
2. 6/3
3. 4/3
4. 9/3

Answer: A

**Section D-(2\*5=10)**

**PROBLEMS (Answer any two)**

**(NOTE: SECTION D: -You should write answer in A4 sheets, scan your answers and save it as a single PDF file withfilename:your Register Number)**

1) Compute the Multiplicationof (-14) and (-5) using Booths Algorithm (5 marks)

2) Carry out themultiplication of (15) and (12) using shift add multiplier (5 marks)

3) Divide 12 by 5 using non restoring division methods (5 marks)

4) Perform Carry Save Addition for the following numbers

1001,1101,1110,1111,1010,1100. Compute sum and carry as result. (5 Marks)